



STIC Search Report

EIC 2800

STIC Database Tracking Number: 154476

TO: Drew Hirshfeld
Location: JEF-9A11
Art Unit : 2854
Friday, May 27, 2005

Case Serial Number: 10/633,386

From: Jeff Harrison
Location: EIC 2800
JEF-4B68
Phone: 22511

Search Notes

Please find attached the search history and the edited search results from EAST, including 716/5 and 716/6, and INSPEC.

I recommend that you browse all the attached results, especially the patents. It is not obvious that I found art (with a second design verification test and the specified circuit events) better than the item you found.

If you would like more searching on this case, or if you have questions or comments, please let me know.

Respectfully,
Jeff Harrison

2/9/5

DIALOG(R) File 2:INSPEC

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7344572 INSPEC Abstract Number: B2002-09-1265B-061, C2002-09-5120-025

Title: Selection and testing of set of hard to detect faults

Author(s): Janciukas, M.

Author Affiliation: Programu inzinerijos katedra, Kaunas Univ. of Technol., Lithuania

Journal: Elektronika ir Elektrotechnika no.4 p.79-83

Publisher: Kauno Technol. Univ,

Publication Date: 2002 Country of Publication: Lithuania

CODEN: ELELFB ISSN: 1392-1215

SICI: 1392-1215(2002)4L.79:STHD;1-K

Material Identity Number: G267-2002-004

Language: Lithuanian Document Type: Journal Paper (JP)

Treatment: Practical (P); Theoretical (T); Experimental (X)

Abstract: Problems of hard-to-detect faults in synchronous sequential circuits are discussed and methods of selecting and testing these faults are analyzed. For **testing**, this method uses an **iterative** model (IM) of the sequential circuit, a modification of the IM and a combinative automatic test pattern generator (**ATPG**). Two methods of **test improvement** are presented: use of the legal and illegal states of the sequential circuit; increased controllability of this circuit by means of additional logic. The method presented guarantees **100% test quality** for all synchronous sequential circuits, i.e. **all hard-to detect faults are tested** and if there are untested faults, they are proven to be undetectable. ITC'99 benchmarks are used in experiments. The results of this work are summarized and conclusions are drawn. (5 Refs)

Subfile: B C

Descriptors: automatic test equipment; **automatic test pattern generation**; circuit testing; fault diagnosis; iterative methods; logic testing; sequential circuits

Identifiers: hard-to-detect faults; synchronous sequential circuits; fault selection; fault testing; sequential circuit iterative model; combinative automatic test pattern generator; **ATPG**; illegal states; legal states; test quality; untested faults; undetectable faults; ITC'99 benchmarks

Class Codes: B1265B (Logic circuits); B1265A (Digital circuit design, modelling and testing); B7210A (Automatic test systems); C5120 (Logic and switching circuits); C7410H (Computerised instrumentation); C5210 (Logic design methods)

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15/9/2

DIALOG(R) File 2:INSPEC

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6631672 INSPEC Abstract Number: B2000-08-2570A-024, C2000-08-7410D-034

Title: Tool vendors take aim at functional **verification**

Author(s): Bassak, G.

Journal: EDN (US Edition) vol.45, no.8 p.101-6

Publisher: Cahners Publishing,

Publication Date: 13 April 2000 **Country of Publication:** USA

CODEN: EDNEFD ISSN: 0012-7515

SICI: 0012-7515(20000413)45:8L.101:TVTF;1-6

Material Identity Number: G340-2000-011

Language: English Document Type: Journal Paper (JP)

Treatment: Applications (A); Practical (P)

Abstract: Spiralling chip and system complexity has pushed functional **verification** to absorb as much as 70% of a chip's **design** effort. To speed chip debugging, vendors are **coupling** simulators with sophisticated test bench-generation and **fault-finding** tools. **Designers** turn to static-analysis tools, such as lint-checking, code-coverage, and emerging formal-**verification** techniques, to slash simulator and synthesis **iterations**. (0 Refs)

Subfile: B C

Descriptors: **fault diagnosis**; formal **verification**; integrated **circuit design**; integrated **circuit testing**; **iterative** methods

16/9/34

DIALOG(R) File 2:INSPEC

(c) Institution of Electrical Engineers. All rts. reserv.

6228558 INSPEC Abstract Number: B1999-06-1265F-004, C1999-06-5130-002

Title: High-level **design verification** of microprocessors via
error modeling

Author(s): Van Campenhout, D.; Al-Asaad, H.; Hayes, J.P.; Mudge, T.;
Brown, R.B.

Author Affiliation: Michigan Univ., Ann Arbor, MI, USA

Journal: ACM Transactions on Design Automation of Electronic Systems
vol.3, no.4 p.581-99

Publisher: ACM,

Publication Date: Oct. 1998 Country of Publication: USA

CODEN: ATASFO ISSN: 1084-4309

SICI: 1084-4309(199810)3:4L.581:HLDV;1-S

Material Identity Number: F110-1999-003

U.S. Copyright Clearance Center Code: 1084-4309/99/1000-0581\$5.00

Language: English Document Type: Journal Paper (JP)

Treatment: Applications (A); Practical (P); Experimental (X)

Abstract: A **design verification** methodology for microprocessor hardware based on modeling **design** errors and generating simulation vectors for the modeled errors via physical **fault testing** techniques is presented. We have systematically collected **design** error data from a number of microprocessor **design** projects. The error data is used to derive error models suitable for **design verification testing**. A class of basic error models is identified and shown to yield **tests** that provide good coverage of common error types. To improve coverage for more complex errors, a new class of conditional error models is introduced. An experiment to evaluate the **effectiveness** of our methodology is presented. Single actual **design** errors are injected into a correct **design**, and it is determined if the **methodology will generate a test that detects the actual errors**. The experiment has been conducted for two microprocessor **designs** and the results indicate that very high coverage of actual **design** errors can be obtained with **test sets** that are complete for a small number of synthetic error models. (32 Refs)

16/9/38

DIALOG(R) File 2:INSPEC

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6147315 INSPEC Abstract Number: B1999-03-1265B-021, C1999-03-5210-007

Title: Generation of **tests** for the localization of single gate **design** errors in combinational circuits using the stuck-at **fault** model

Author(s): Ubar, R.; Borrione, D.

Author Affiliation: Univ. Joseph Fourier, Grenoble, France

Conference Title: Proceedings. XI Brazilian Symposium on Integrated Circuit Design (Cat. No.98EX216) p.51-4

Editor(s): Lubaszewski, M.; Alves, C.A.

Publisher: IEEE Comput. Soc, Los Alamitos, CA, USA

Publication Date: 1998 Country of Publication: USA xv+250 pp.

ISBN: 0 8186 8704 5 Material Identity Number: XX-1998-02671

U.S. Copyright Clearance Center Code: 0 8186 8704 5/98/\$10.00

Conference Title: Proceedings. XI Brazilian Symposium on Integrated Circuit Design (Cat. No.98EX216)

Conference Sponsor: Brazilian Comput. Soc. (SBC); Brazilian Microelectron. Soc. (SBMicro)

Conference Date: 30 Sept.-3 Oct. 1998 Conference Location: Rio de Janeiro, Brazil

Language: English Document Type: Conference Paper (PA)

Treatment: Theoretical (T); Experimental (X)

Abstract: We propose a new approach to generate diagnostic **tests** and localize single gate **design** errors in combinational circuits. The method is based on using the stuck-at **fault** model with subsequent translation of the diagnosis into the **design** error area. This allows to exploit standard gate-level ATPGs for **verification** and **design** error diagnosis purposes. A powerful hierarchical approach is proposed for **generating test patterns**, which, at first, localize the **faulty** macro (tree-like subcircuit), and then localize the erroneous gate in the **faulty** macro. Experimental data show the efficiency of the macro-level test generation and **fault** simulation compared to the plain gate-level approaches. (9 Refs)

10/9/4

DIALOG(R) File 2:INSPEC

(c) Institution of Electrical Engineers. All rts. reserv.

7637107 INSPEC Abstract Number: B2003-06-1265A-079, C2003-06-5210B-037

Title: ATPG system and fault simulation methods for digital devices

Author(s): Hahanov, V.; Pudov, V.; Sysenko, I.

Author Affiliation: Kharkov Nat. Univ. of Radio Electron., Ukraine

Conference Title: Programmable Devices and Systems 2001 (PDS 2001).

Proceedings volume from the 5th IFAC Workshop p.263-7

Editor(s): Hrynkiewicz, W.C.E.; Klosowski, P.

Publisher: Elsevier Sci, Kidlington, UK

Publication Date: 2002 **Country of Publication:** UK **ix+309 pp.**

ISBN: 0 08 044081 9 Material Identity Number: XX-2003-00126

Conference Title: Programmable Devices and Systems 2001. Proceedings
volume from the 5th IFAC Workshop

Conference Sponsor: IFAC

Conference Date: 22-23 Nov. 2001 Conference Location: Gliwice, Poland

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P); Theoretical (T)

Abstract: Models and methods of digital **circuit** analysis for test generation and fault simulation are offered. A two-frame cubic algebra for a compact description of sequential primitive elements (here and further, primitive), in the form of cubic coverings, is used. Digital **circuit** testing problems are formulated as linear equations. The described cubic fault simulation method allows the propagation of a primitive fault list from its inputs to outputs; to generate analytical equations for deductive fault simulation of digital circuits at gate, functional and algorithmic description levels; to build compilative and interpretative fault simulators for digital circuits. Fault list cubic coverings (FLCC), which allow the creation of single sensitization paths, are proposed. The test generation method for single stuck-at fault (SSF) detection with the usage of FLCC is developed. The means of test generation for digital devices designed in Active-HDL are offered. The design input description is based on the usage of VHDL, Verilog and graphical representations of finite state machines (FSM). The obtained **tests** are used for digital **design verification** in Active-HDL. For fault coverage evaluation, the program implementation of cubic simulation method is used. (7 Refs)

Subfile: B C

Descriptors: automatic test pattern generation; circuit CAD;
fault diagnosis; fault simulation; finite state machines; hardware
description languages; integrated **circuit** design; integrated
circuit testing; linear algebra; logic CAD; logic testing

DERWENT-ACC-NO: 1996-455627

DERWENT-WEEK: 200317

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TITLE: Pseudo-random instruction generating system for microprocessor design verification and test system - generates text for sequence of assembly language instructions by mixing text instructions generated by pre-programmed operations from at least two test generators

INVENTOR: WHITMAN, J D

PATENT-ASSIGNEE: SUN MICROSYSTEMS INC[SUNM]

PRIORITY-DATA: 1995US-0412157 (March 28, 1995)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
DE 69625474 E	January 30, 2003	N/A	000	G06F 011/263
WO 9630834 A1	October 3, 1996	E	034	G06F 011/263
US 5572666 A	November 5, 1996	N/A	020	G06F 011/34
EP 818002 A1	January 14, 1998	E	000	G06F 011/263
JP 11508710 W	July 27, 1999	N/A	051	G06F 011/22
EP 818002 B1	December 18, 2002	E	000	G06F 011/263

DESIGNATED-STATES: JP AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE DE FR
GB DE FR GB

CITED-DOCUMENTS: DE 3418360; DE 3921628 ; US 4339819

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
DE 69625474E	N/A	1996DE-0625474	March 27, 1996
DE 69625474E	N/A	1996EP-0910631	March 27, 1996
DE 69625474E	N/A	1996WO-US04264	March 27, 1996
DE 69625474E	Based on	EP 818002	N/A
DE 69625474E	Based on	WO 9630834	N/A
WO 9630834A1	N/A	1996WO-US04264	March 27, 1996
US 5572666A	N/A	1995US-0412157	March 28, 1995
EP 818002A1	N/A	1996EP-0910631	March 27, 1996
EP 818002A1	N/A	1996WO-US04264	March 27, 1996
EP 818002A1	Based on	WO 9630834	N/A
JP 11508710W	N/A	1996JP-0529646	March 27, 1996
JP 11508710W	N/A	1996WO-US04264	March 27, 1996
JP 11508710W	Based on	WO 9630834	N/A
EP 818002B1	N/A	1996EP-0910631	March 27, 1996
EP 818002B1	N/A	1996WO-US04264	March 27, 1996
EP 818002B1	Based on	WO 9630834	N/A

INT-CL (IPC): G06F011/00, G06F011/22 , G06F011/263 , G06F011/273 ,
G06F011/34

ABSTRACTED-PUB-NO: US 5572666A

BASIC-ABSTRACT:

The test system generates a processor instruction text file containing a sequence of instructions in a target processor's assembly language, by intermixing assembly language instructions provided from at least two sources. The sources (test generators) are programs which program various operations into a 'test interpreter', which interprets the operations by pseudo-randomly mixes the assembly language instructions specified by the various test generators to output a 'processor instruction text' file containing a sequence of assembly language instructions for running on the target processor.

The 'test generators' may be programmed to contain blocks of operations which must be interpreted back-to-back, without mixing between multiple test generators, such that the processor instruction text files includes instruction sequences specifically tailored to a user's requirements.

USE - Generating pseudo-random instructions for design verification of microprocessors.

ADVANTAGE - Provides self checking constructs used to compare processor's results with expected results.

ABSTRACTED-PUB-NO: WO 9630834A

EQUIVALENT-ABSTRACTS:

A system for outputting a sequence of processor instructions for execution on a target processor, the system comprising:

at least two executable test generators which when executed specify particular processor instructions to be used in said sequence of processor instruction for execution on said target processor; and

a test interpreter which at least partially shuffles the particular processor instructions from said at least two independent test generators and generates said sequence of processor instructions for execution on said target processor such that sequence includes two of said particular processor instructions from one test generator which are separated from one another by one or more particular processor instructions from the other test generator.

CHOSEN-DRAWING: Dwg.3/9 Dwg.1/9

TITLE-TERMS: PSEUDO RANDOM INSTRUCTION GENERATE SYSTEM MICROPROCESSOR DESIGN
VERIFICATION TEST SYSTEM GENERATE TEXT SEQUENCE ASSEMBLE LANGUAGE
INSTRUCTION MIX TEXT INSTRUCTION GENERATE PRE PROGRAM OPERATE TWO
TEST GENERATOR

DERWENT-CLASS: T01

EPI-CODES: T01-F05A; T01-G02A2D;

SECONDARY-ACC-NO:

Non-CPI Secondary Accession Numbers: N1996-383877



STIC EIC 2800

Search Request Form

Today's Date:

5/26/05

What date would you like to use to limit the search?

Priority Date: 8/1/03

Other:

Name Drew Hirshfeld
AU 2854 Examiner # 72421
Room # 9A11 Phone 22168
Serial # 10633386

Format for Search Results (Circle One):

PAPER DISK EMAIL

Where have you searched so far?

USPAT DWPI EPO JPO IBM TDB

IEEE INSPEC Other _____

Is this a "Fast & Focused" Search Request? (Circle One) YES NO

Please request a "Fast & Focused" search in-person at EIC2800, JEF-4B68. A "Fast & Focused" Search is completed in 2 hours (maximum). The search must be on a very specific topic and meet certain criteria. The criteria are posted in EIC2800 and on the EIC2800 NPL Web Page at <http://ptoweb/patents/stic/stic-tc2800ffcriteria.htm>

What is the topic, novelty, motivation, utility, or other specific details defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, definitions, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract, background, brief summary, pertinent claims and any citations of relevant art you have found.

- Characterize an Electronic Circuit
- Events, faults, noise, hazard
- Test Method
- See attached R.I.F.
- Second design verification test

STIC Searcher

Harrison

Phone

22511

Date picked up

5/26/05

Date Completed

5/27/05



Histories

10/633,386

27may05 15:46:00 User259284 Session D3187.6

File 2:INSPEC 1969-2005/May W3
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Set	Items	Description
S1	2294	TEST?????? (4N) VERIF??????? (8N) DESIGN?????
S2	8742	EVALUAT?????? (4N) EFFECTIVE????????
S3	7	1AND2
S4	2	DESIGN() TEST() VERIFICATION
S5	1257	S1:S4 AND CIRCUIT
S6	4	S5 AND EXERCIS?????? (4N) CIRCUIT???????
S7	14047	FAULT DIAGNOSIS (January 1995)
S8	90	S1:S6 AND S7
S9	73	S8 AND TEST?????
S10	13	S8 AND TESTS
S11	7000	TESTING AND S1:S10
S12	1564	S11 AND (VERIF????????? OR VALIDAT?????) AND DESIGN???????
S13	515	S12 AND (FAULT?? OR RACE? ? OR NOISE? ? OR EVENT? ? OR DYN- AMIC OR HAZARD? ? OR COUPLING? ?)
S14	338	S13 AND CIRCUIT????
S15	5	S14 AND ITERAT???????????
S16	89	S13 AND TESTS

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3234	(716/4 or 716/5 or 716/6).ccls.	US-PGPUB; USPAT	OR	OFF	2005/05/27 13:00
L2	11	L1 and dynamic\$4 near3 (event or hazard\$6)	US-PGPUB; USPAT	OR	ON	2005/05/27 12:23
L3	537	L1 and (race\$4 or time\$2 or timing\$2) near2 (test\$5 or event)	US-PGPUB; USPAT	OR	ON	2005/05/27 12:26
L4	97	L1 and coupl\$3 near2 (test\$5 or event)	US-PGPUB; USPAT	OR	ON	2005/05/27 12:25
L5	77	L1 and (noise or ((spurious\$3 or random\$%) near2 signal\$3)) near3 (occur\$7 or test\$5 or event)	US-PGPUB; USPAT	OR	ON	2005/05/27 12:26
L6	512	L1 and ((2nd or additional or another or second) adj2 (design or verification or validation or evaluation or test))	US-PGPUB; USPAT	OR	ON	2005/05/27 12:28
L7	320	L1 and (2nd or additional or another or second) adj3 design	US-PGPUB; USPAT	OR	ON	2005/05/27 12:29
L8	102	L1 and (2nd or additional or another or second) adj3 (verification or validation)	US-PGPUB; USPAT	OR	ON	2005/05/27 12:29
L9	358	L1 and (2nd or additional or another or second) adj3 (test or testing or evaluation or evaluating)	US-PGPUB; USPAT	OR	ON	2005/05/27 12:30
L10	8	L7 and L8 and L9	US-PGPUB; USPAT	OR	ON	2005/05/27 12:31
L11	0	L2 and L10	US-PGPUB; USPAT	OR	ON	2005/05/27 12:31
L12	3	L3 and L10	US-PGPUB; USPAT	OR	ON	2005/05/27 12:31
L13	3	L4 and L10	US-PGPUB; USPAT	OR	ON	2005/05/27 12:31
L14	0	L5 and L10	US-PGPUB; USPAT	OR	ON	2005/05/27 12:32
L15	26	L6 and (L3 and L4)	US-PGPUB; USPAT	OR	ON	2005/05/27 12:32
L16	3	L6 and (L3 and L5)	US-PGPUB; USPAT	OR	ON	2005/05/27 12:32
L17	0	L6 and (L4 and L5)	US-PGPUB; USPAT	OR	ON	2005/05/27 12:33
L18	0	L3 and L4 and L5	US-PGPUB; USPAT	OR	ON	2005/05/27 12:33
L19	52	L3 and L4	US-PGPUB; USPAT	OR	ON	2005/05/27 12:33
L20	11	L3 and L5	US-PGPUB; USPAT	OR	ON	2005/05/27 12:33
L21	2	L4 and L5	US-PGPUB; USPAT	OR	ON	2005/05/27 12:33
L22	80	L10 or L12 Or L13 or L16 or L17 or L18 or L19 or L20 or L21 or L2	US-PGPUB; USPAT	OR	ON	2005/05/27 13:53
L23	32	L2 or L10 or L12 or L13 or L16 or L20 or L21	US-PGPUB; USPAT	OR	ON	2005/05/27 12:49
L24	4	L23 and (test\$4 near2 case)	US-PGPUB; USPAT	OR	ON	2005/05/27 12:49

L25	76	L22 not L24	US-PGPUB; USPAT	OR	OFF	2005/05/27 13:47
L26	3154	L1 not (L22 or L24)	US-PGPUB; USPAT	OR	ON	2005/05/27 13:54
L27	166	L26 and effectiv\$7.clm,ab,ti.	US-PGPUB; USPAT	OR	ON	2005/05/27 14:20
L28	573	716/5.cor.	US-PGPUB; USPAT	OR	ON	2005/05/27 15:22
L29	20	design adj1 verification adj1 test\$5	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:23
L30	8306	(determin\$6 or evaluat\$7) near4 effective\$7	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:23
L31	1	L29 and L30	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:24
L32	397	(L29 or L30) and (T01-J15A1 or T01-J15B or T01-S03 or U11-G03).mc.	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:25
L33	1	(L29 or L30) and (T01-J15A1 and T01-J15B and T01-S03 and U11-G03).mc.	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:28
L34	2	(L29 or L30) and (T01-J15A1 and T01-J15B).mc.	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:25
L35	1	(L29 or L30) and (T01-J15A1 and T01-S03 and U11-G03).mc.	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:28
L36	10	(L29 or L30) and T01-J15A1.mc.	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:27
L37	374	(L29 or L30) and T01-S03.mc.	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:27
L38	14	(L29 or L30) and U11-G03.mc.	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:28
L39	17	(L29 or L30) and T01-J15B.mc.	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:29
L40	392	(L36 or L37 or L38 or L39) and effective\$8	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:29
L41	132	(L36 or L37 or L38 or L39) and evaluat\$8	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:29
L42	59	(L36 or L37 or L38 or L39) and design\$7	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:30
L43	16	(L36 or L37 or L38 or L39) and verif\$8	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:30

L44	24	L40 and L41 and L42	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:31
L45	2577	effective\$7 near2 test\$7	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:32
L46	158	L30 and L45	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:32
L47	16	L46 and (ic or ics or circuit\$3 or dut or dut\$)	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:41
L48	1	L46 and (second or 2nd) adj2 test\$4	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:49
L49	0	L46 and dynamic\$4 near2 hazard\$5	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:42
L50	1	L46 and hazard\$5	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:42
L51	0	L46 and race	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:43
L52	64	test near3 evaluat\$6 near4 effective\$6	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:43
L53	1774	(second or 2nd) adj1 test\$4	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:50
L54	23	(second or 2nd) adj1 validation	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:50
L55	63	(second or 2nd) adj1 verification	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:50
L56	1601	(second or 2nd) adj1 test	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:50
L57	206	(L54 or L55 or L56) and (race or path or hazard or dynamic or coupling or event or noise or crosstalk or (cross adj1 talk))	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:52
L58	83	L57 and circuit	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:52
L59	0	L57 and microcircuit	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:52
L60	13	L58 and (evaluat\$6 or effective\$7)	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:56
L61	240	exercis\$6 near2 circuit\$4	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:56

L62	36	(T01\$ or u11\$ or h01L\$) and L61	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 16:07
L63	2	L30 and L61	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 15:57
L64	99	exercis\$6 near1 circuit	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 16:07
L65	22	effective\$7.ti. and test\$5.ti. and evaluat\$6.ti.	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 16:20
L66	20273	G01R031/02\$	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 16:20
L67	8	L66 and evaluat\$7 near3 effective\$7	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 16:22
L68	0	another adj1 design adj1 verification adj1 test	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 16:23
L69	14	design adj1 verification adj1 test	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/05/27 17:00
L70	573	716/6.cor.	US-PGPUB; USPAT	OR	ON	2005/05/27 17:01